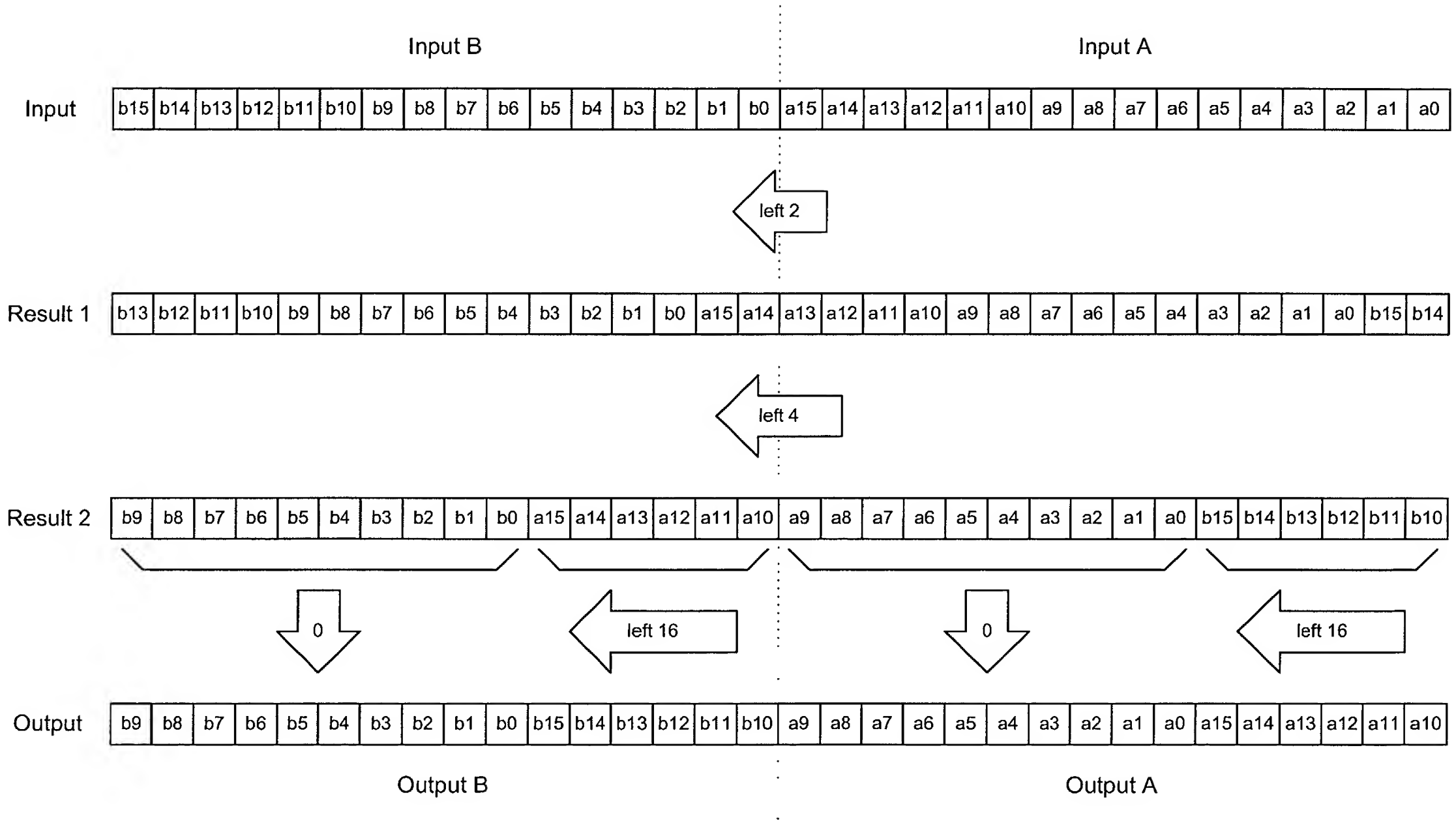

FIGURE 1

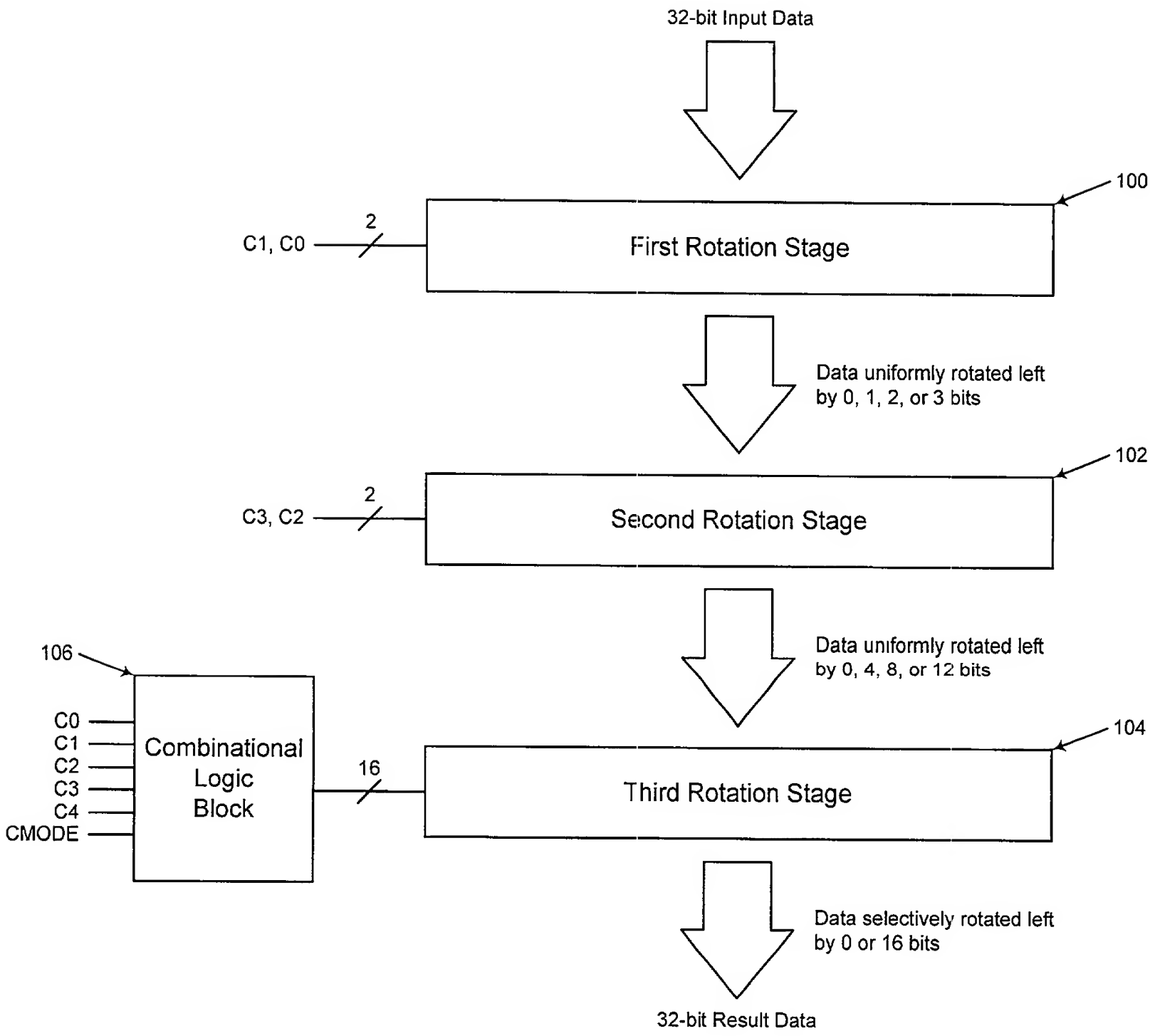
32-bit Input Data
100
C1, C0
2
First Rotation Stage
Data uniformly rotated left
by 0, 1, 2, or 3 bits
102
C3, C2
2
Second Rotation Stage
Data uniformly rotated left
by 0, 4, 8, or 12 bits
106
C0
C1
C2
C3
C4
CMODE
Combinational
Logic
Block
16
104
Third Rotation Stage
Data selectively rotated left
by 0 or 16 bits
32-bit Result Data

FIGURE 2

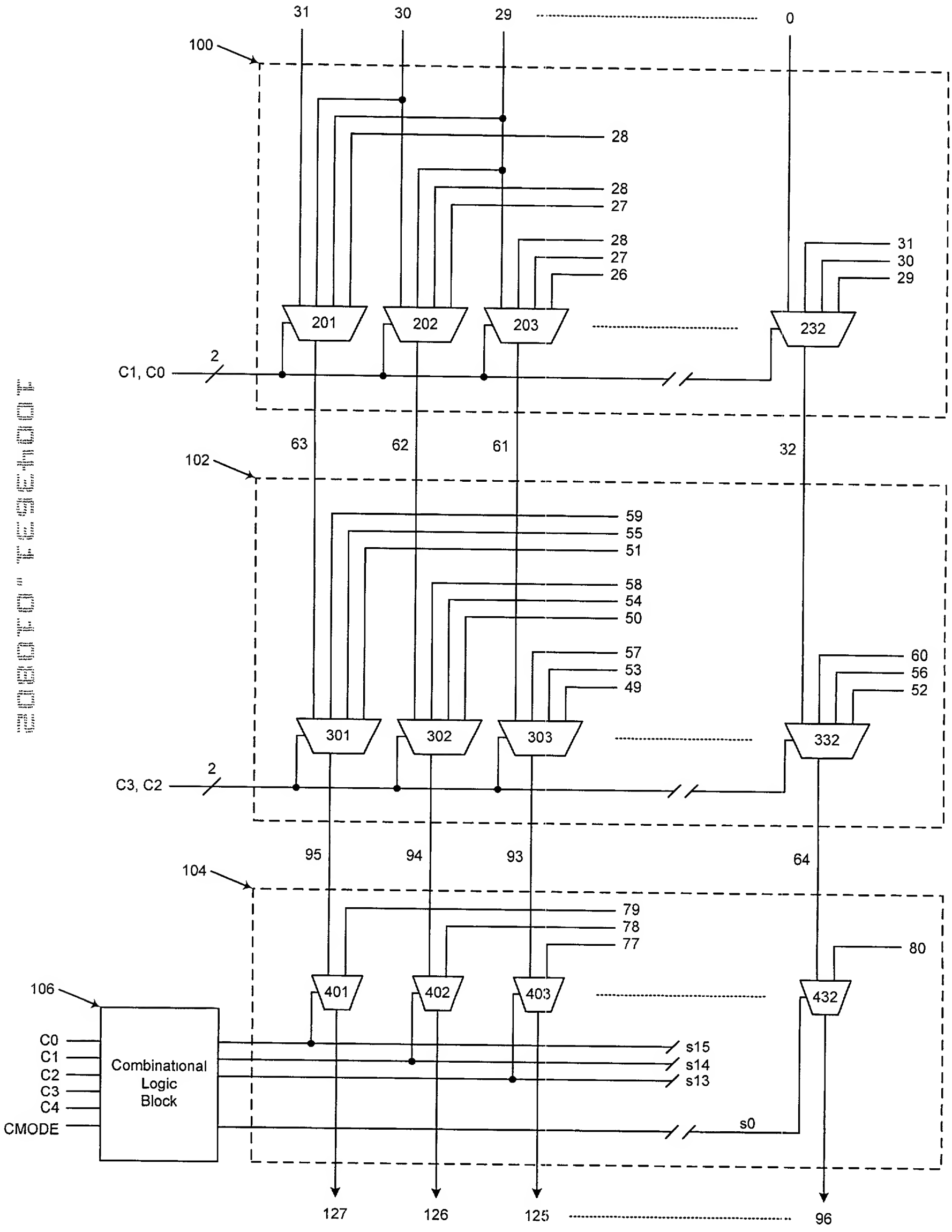
31
30
29
0
100
28
28
27
28
27
26
31
30
29
201
202
203
232
2
C1, C0
63
62
61
32
102
59
55
51
58
54
50
57
53
49
60
56
52
301
302
303
332
2
C3, C2
95
94
93
64
104
79
78
77
80
401
402
403
432
106
C0
C1
C2
C3
C4
CMODE
Combinational Logic Block
s15
s14
s13
s0
127
126
125
96

FIGURE 3

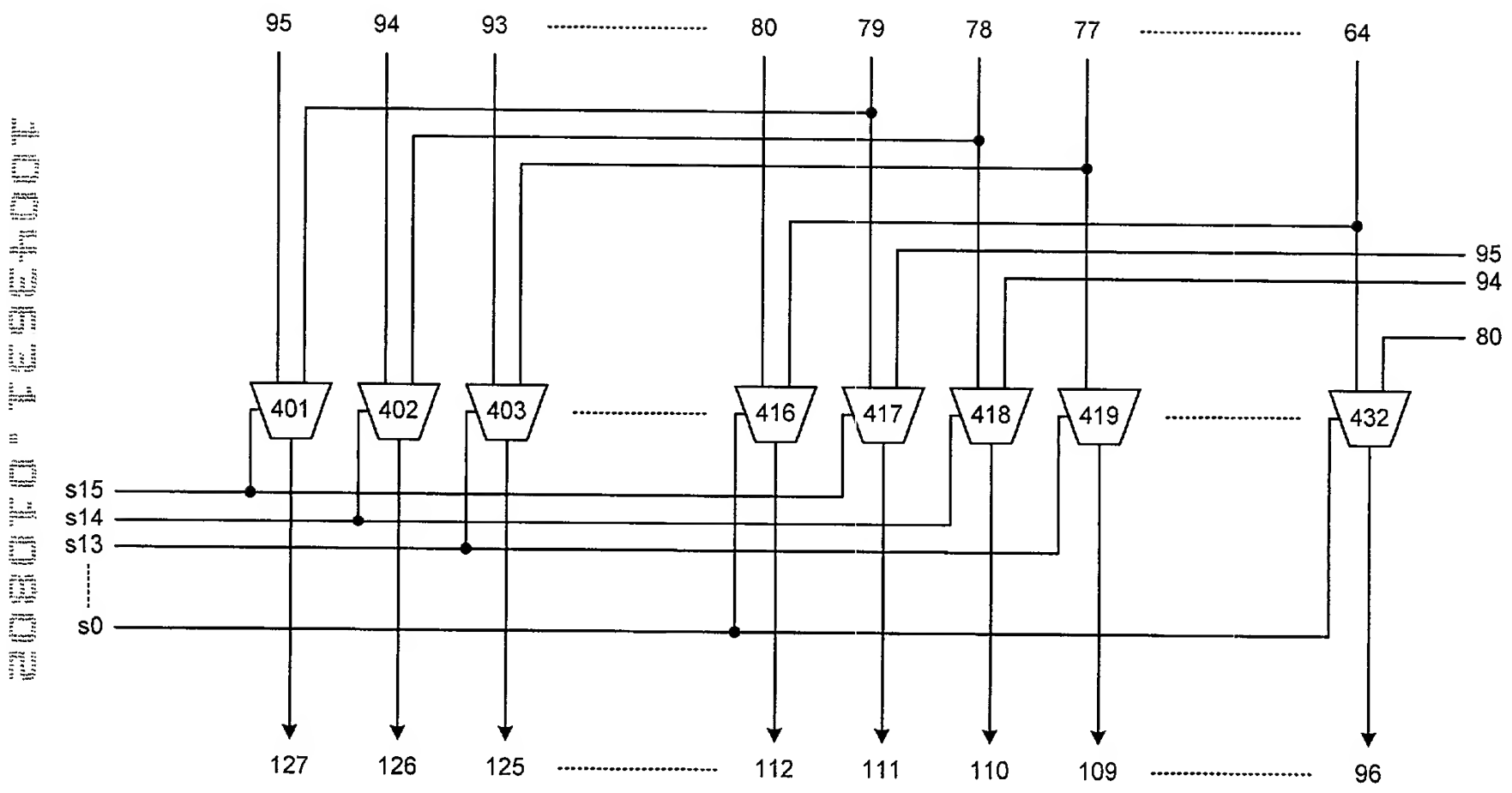
95
94
93
80
79
78
77
64
95
94
80
401
402
403
416
417
418
419
432
s15
s14
s13
s0
127
126
125
112
111
110
109
96

FIGURE 4

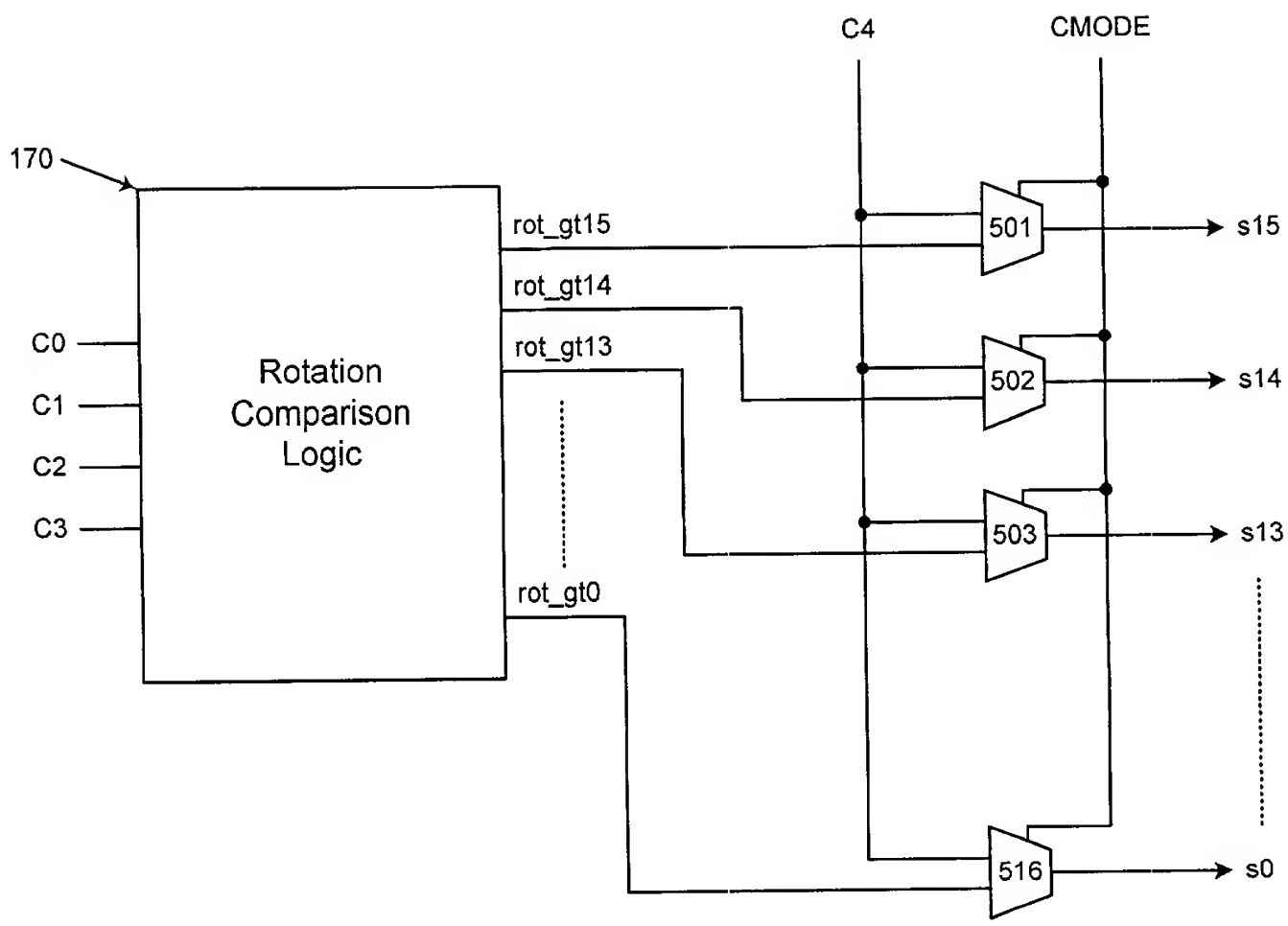
C4
CMODE
170
C0
C1
C2
C3
Rotation
Comparison
Logic
rot_gt15
rot_gt14
rot_gt13
rot_gt0
501
502
503
516
s15
s14
s13
s0

FIGURE 5